REMARKS

The Final Office Action dated June 25, 2004 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

As a preliminary matter, Applicant thanks Examiner Joe Logsdon for conducting a personal interview with Applicant's representative, Hermes M. Soyez, on September 7, 2004.

Upon entry of this Response, claims 1-22 will be pending in the present application. Claims 1-2, 5-6, 8-11, 13, 15-18, 20, and 22 are independent claims. Claims 1-2, 5-6, 8-11, 13, 15-18, 20, and 22 have been amended to more particularly point out and distinctly claim the present invention. Claims 2, 5-6, 8-9, 11, 15-16, 18, and 22 have merely been placed in independent form. Support for the subject matter added to claims 1, 10, 13, 17, and 20 may be found at least on page 63, lines 1-2, of the specification of the present application. No new matter has been added. Claims 1-22 are respectfully submitted for consideration.

Rejection of Claim 1, 10, 13-14, 17, and 19-21 Under 35 U.S.C. § 103(a):

Claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,239,381 to Takahashi (Takahashi '381) in view of U.S. Patent No. 6,275,546 B1 to Miller et al. (Miller '546). In the Office Action, it was acknowledged that Takahashi '381 fails to disclose that the write clock signal is a glitchless fractional clock pulse. However, it was alleged in the Office Action that Miller '546 may be

combined with Takahashi '381 to yield the claimed invention. This rejection is respectfully traversed.

Claims 10, 13-14, 17, and 19-21 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Miller '546 in view of Takahashi '381. In the Office Action, it was acknowledged that Miller '546 fails to disclose transmitting a glitchless fractional clock pulse to a gate input of a latch to enable the latch to store data during an optimally stable period. However, it was alleged in the Office Action that Takahashi '381 may be combined with Miller '546 to yield the claimed invention. This rejection is respectfully traversed.

Claim 1, upon which claims 2-9 depend, recites a method for storing data. The method includes generating a glitchless fractional clock pulse in a circuit, transmitting the glitchless fractional clock pulse from the circuit to a data storage element, and storing data in the storage element upon receiving the glitchless fractional clock pulse.

Claim 10, upon which claims 11-12 depend, recites a method for enabling a latch. The method includes receiving a clock signal in a logic circuit, receiving a latch enable pulse in the logic circuit, generating a glitchless fractional clock pulse in the logic circuit in response to the latch enable pulse and the clock signal, and transmitting the glitchless fractional clock pulse to a gate input of a latch to enable the latch to store data during an optimally stable time period.

Claim 13, upon which claims 14-16 depend, recites an apparatus for storing data. The apparatus includes at least one storage element having a data input, a storage enable

input, and a data output, and at least one logic circuit having an activating input, an clock input, and a logic output. The at least one logic circuit generates a glitchless fractional clock pulse on the logic output, the logic output being connected to the storage enable input of the storage element and operating to enable the at least one storage element to store data resident on the data input at an optimally stable time

Claim 17, upon which claims 18 and 19 depend, recites a network switch for switching data. The network switch includes at least one data port interface, at least one storage element in connection with the at least one data port interface and having a data input, a storage enable input, and a data output, and at least one logic circuit having an activating input, a clock input, and a logic output. The at least one logic circuit is configured to generate a glitchless fractional clock pulse on the logic output, the logic output being connected to the storage enable input of the storage element and operating to enable the at least one storage element to store data resident on the data input at an optimally stable time.

Claim 20, upon which claims 21 and 22 depend, recites an apparatus for storing data. The apparatus includes a storage means for storing data, the storage means having an input for receiving data to be stored, a storage enable input for enabling the storage means, and a data output. The apparatus also includes at least one pulse generating means for generating a glitchless fractional clock pulse, the pulse generating means having an activating input, a clock input, and an output in connection with the storage enable input of the storage means. The pulse generating means generates the glitchless

fractional clock pulse that is transmitted to the storage means to enable the storage means to store data at an optimally stable time.

As discussed in the present specification, the claimed invention allows for storage of data during a predictably stable portion of a clock cycle and also minimizes overhead consumption. It is respectfully submitted that Takahashi '381 and Miller '546, taken either individually or in combination, fail to disclose or suggest the elements of any of the presently pending claims and therefore fail to provide the advantages of the claimed invention.

Takahashi '381 discloses "an apparatus for recording and reproducing a video signal by using rotary heads" (column 1, lines 7-9). Takahashi '381, in claim 1 thereof, also discloses "means for controlling the buffer memory to store the effective video period of each of a predetermined number of scanning line periods per frame period selected from the plurality of scanning line periods per frame period of the first digital video signal in response to the at least one write clock signal".

However, Takahashi '381 fails to disclose or suggest at least "generating a glitchless fractional clock pulse in a circuit...wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse", as recited in claims 1-12 of the present application. Also, Takahashi '381 fails to disclose or suggest at least "at least one logic circuit" that generates "a glitchless fractional clock pulse...wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse", as recited in claims 13-19. In addition, Takahashi '381 fails to disclose or suggest at least

"at least one pulse generating means for generating a glitchless fractional clock pulse...wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse", as recited in claims 20-22.

Miller '546 discloses "electrical circuitry for producing an output clock signal that is selectively synchronized to one of two generally free-running input clock signals" (column 1, lines 58-60). Miller '546 also discloses that one of its primary objects is "to provide an improved clock switching apparatus which prevents glitches in the resulting output clock signal" (column 1, lines 36-38). As such, Miller '546 further discloses "switching between the input clock signals in a manner whereby the output clock signal does not have any clock pulses that are shrunk or narrowed" (column 1, lines 61-63).

However, like Takahashi '381, Miller '546 also fails to disclose or suggest at least "generating a glitchless fractional clock pulse in a circuit...wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse", "at least one logic circuit" that generates "a glitchless fractional clock pulse... wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse", and "at least one pulse generating means for generating a glitchless fractional clock pulse... wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse", as recited in the currently pending claims of the present application.

On page 2 of the Office Action, it is alleged that the specification of the present application does not provide a definition for "fractional". It is further alleged in the Office Action that any glitchless clock pulse is a glitchless fractional clock pulse.

In the Response dated April 1, 2004, Applicant indicated his disagreement with the above allegations and pointed out that a definition of "fractional" may be found from page 62, line 28, to page 63, line 11, of the specification of the present application. Applicant also pointed out that Figure 32 of the present application illustrated a glitchless fractional clock pulse in the waveform labeled "Gate[i]". However, in the Response to Arguments section of the Final Office Action, it was alleged that the above-mentioned portion of the present specification fails to describe how a "glitchless fractional clock pulse" differs from a "glitchless clock pulse". It was also alleged that Figure 32 of the present application does not reveal the meaning of "fractional".

In view of the above amendments to the claims, Applicant respectfully points out that the "glitchless fractional clock pulse" recited in claims 1-22 differs from a "glitchless clock pulse" at least because, as recited in claims 1-22, the "glitchless fractional clock pulse is of a shorter period than a system core clock pulse".

In addition, Applicant respectfully points out that Miller '546 discloses that a common problem associated with switching from one clock to another is that a clock pulse width at or near the switching operation will be shrunk (column 1, lines 26-28). Miller '546 also discloses that such narrower than standard pulse widths or shorter clock periods are defined as "glitches" (column 1, lines 34-35). Therefore, one of skill in the art understands that glitchless clock pulses are those pulses that have not been shortened by a switching operation, and that are of the same width as the standard clock pulse.

Further, at the top of Figure 32 of the present application, a general clock signal, CLK, is illustrated. The CLK waveform includes a set of pulses, each having the same "standard" width. At the bottom of Figure 32, a Gate[i] signal is illustrated. The Gate[i] waveform includes a representative "glitchless fractional clock pulse" according to the claimed invention. As illustrated in Figure 32, the width of the Gate[i] pulse is narrower than the width of the CLK pulses. Also, as explained on lines 1-2 of page 63 of the present specification, glitchless clock pulses are "generally of a shorter period than the system core clock pulse". However, the shorter period of the Gate[i] pulse is not due to a "glitch". At least in view of the above, it is respectfully submitted that "fractional" is sufficiently defined in the present application to enable one of skill in the art to practice the claimed invention. It is also re-asserted that Miller '564 and Takahashi '381 both fail to disclose or suggest the "glitchless fractional clock pulse" recited in claims 1-22 of the present application.

At least in view of the above, reconsideration and withdrawal of the rejection of claim 1 as being unpatentable over Takahashi '381 in view of Miller '564 and of claims 10, 13-14, 17, and 19-21 as being unpatentable over Miller '564 in view of Takahashi '381 is respectfully requested.

Allowable Subject Matter:

Claims 2-6, 8-9, 11-12, 15-16, 18, and 22 were objected to as being dependent upon rejected base claims. However, claims 2-6, 8-9, 11-12, 15-16, 18, and 22 were acknowledged in the Office Action to recite allowable subject matter. Applicant thanks

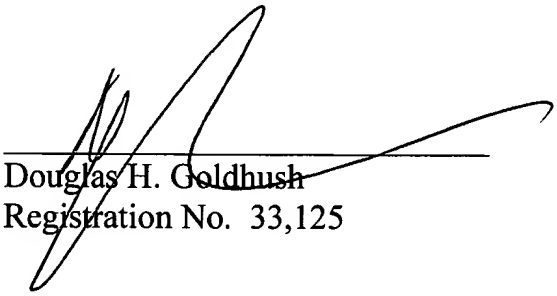
the Examiner for this acknowledgement. Applicant also points out that claims 2-6, 8-9, 11-12, 15-16, 18, and 22 no longer depend upon rejected base claims. Therefore, allowance of claims 2-6, 8-9, 11-12, 15-16, 18, and 22 is respectfully requested.

Applicant respectfully submits that all of the issues raised in the Office Action have been addressed and that all of the rejections included in the Office Action have been overcome. Applicant further submits that, at least in view of the above, claims 1-22 of the present application contain allowable subject matter. Therefore, it is respectfully requested that all claims pending in the present application be allowed and that this application be passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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